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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/667,615	09/22/2003	Theodore W. Houston	TI 35657	1175

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EXAMINER	
OWENS, DOUGLAS W	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 05/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/667,615	HOUSTON, THEODORE W.	
	Examiner	Art Unit	
	Douglas W. Owens	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 2/8/05.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-20 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1,5-7,10,11,13,15,17 and 20 is/are rejected.

7)☒ Claim(s) 2-4,8,9,12,14,16,18 and 19 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 2/8/05.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 5, 6, 7, 10, 13 and 15 are rejected under 35 U.S.C. 102(e) as being anticipated by US Patent No. 6,720,619 to Chen et al.

Regarding claim 1, Chen et al. teach a transistor (Figs. 1(c) and 2, for example) comprising:

a body region insulated from a substrate;

an insulating layer (the gate dielectric) on a surface of the body region; and

a gate structure on the insulating layer and conformally surrounding a portion of the body region, wherein a width of the body region is sufficient to provide a not fully depleted region (Col. 3, lines 47 – 57; Col. 4, lines 29 – 34; Col. 6, lines 6 – 18).

Regarding claims 5 and 6, Chen et al. teach a transistor, wherein the body region is insulated from the substrate by an oxide layer (Buried Oxide; Col. 2, lines 52 – 61).

Regarding claim 7, Chen et al. teach a method of making a transistor (Figs. 1(c) and 2), comprising:

forming a body region insulated from a substrate;

depositing an insulating layer (Col. 4, lines 48 – 50) on a surface of the body region; and

forming a gate structure on the insulating layer and conformally surrounding a portion of the body region, wherein a width of the body region is sufficient to provide a not fully depleted region.

Regarding claim 10, Chen et al. teach a method of making a transistor, wherein the body region is formed from an SOI substrate (Col. 2, lines 52 – 61).

Regarding claim 13, Chen et al. teach a method, wherein the gate structure is a tri-gate.

Regarding claim 15, Chen et al. teach a method, wherein the gate structure is a FIN-FET.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al. as applied to claims 7 and 10 above, and further in view of US Patent No. 6,720,231to Fried et al.

Chen et al. do not teach a method, wherein forming the body region includes forming a mask by depositing and patterning a resist over the silicon layer and performing an anisotropic etch to remove portions of the silicon layer not protected by

the mask. Fried et al. teach a method of forming a body region including forming a mask by depositing and patterning a resist over the silicon layer and performing an anisotropic etch to remove portions of the silicon layer not protected by the mask (Col. 4, lines 23 – 36). It would have been obvious to one of ordinary skill in the art to incorporate the method taught by Fried et al. into the method of Chen et al., since it is desirable to use known and reliable methods of patterning semiconductor layers.

5. Claims 17 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al. in view of US Patent Application Publication No. 2004/0169239 to Rim.

Regarding claim 17, Chen et al. teach a transistor (Figs. 1(c) and 2, for example) comprising:

a body region insulated from a substrate;

an insulating layer (the gate dielectric) on a surface of the body region; and

a gate structure on the insulating layer and conformally surrounding a portion of the body region, wherein a width of the body region is sufficient to provide a not fully depleted region.

Chen et al. do not teach a transistor including a logic transistor and interconnects to the logic transistor to form an operative integrated circuit. Rim teaches a logic circuit comprising interconnected FinFET devices (Paragraph [0026]). It would have been obvious to one of ordinary skill in the art to incorporate the teaching of Rim into the device taught by Chen et al., since it is desirable to add functionality to the device, which can be achieved with the logic circuitry.

Regarding claim 20, neither Chen et al. nor Rim explicitly teach a device, wherein the body region of the logic transistor is fully depleted. Chen et al. teach a device, wherein body regions of transistors are fully depleted (FD-SOI; Col. 1, lines 34 – 39). It would have been obvious to one of ordinary skill in the art to use fully depleted transistors for the logic transistors instead of partially depleted transistors, since partial depletion transistors are subject to variations in the body potential (Col. 1, lines 53 – 57) during transient device operation.

It would have been obvious to incorporate the teaching of Rim into the device taught by Chen et al. for reasons discussed above.

Allowable Subject Matter

6. Claims 2 – 4, 8, 9, 12, 14, 16, 18 and 19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

7. Applicant's arguments filed February 8, 2005 have been fully considered but they are not persuasive.

Applicant argues that Chen et al. only teach only the use fully-depleted devices. The claims do not preclude the use of fully-depleted devices, only that a width of a body region is sufficient to provide a not fully depleted region. Chen et al. teach that partial depletion technology can be used to make fully depleted devices by making other adjustments aside from the width of the body region (Col. 3, lines 47 – 57). Moreover,

Chen et al. also teach forming partially depleted devices (Col. 2, lines 54 – 61; Col. 4, lines 28 – 35).

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

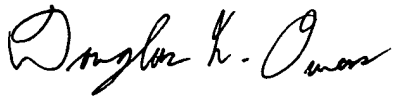
A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Douglas W. Owens whose telephone number is 571-272-1662. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Douglas W Owens
Examiner
Art Unit 2811

DWO